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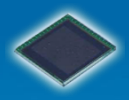
PK9210K 2.0MP Product Brief



The PK9210K has excellent noise performance for low light condition and high dynamic range support by 2-exp line based HDR mode up to 120dB

The PK9210K is the 1/2.92" RGB bayer CMOS image sensor (CIS) designed to support 2.0MP at 30 frames per second (fps).
The PK9210K consists of 1960 (H) x 1120 (V) effective pixels with 12 added active pixels on each side and 8 pixels on each side for color interpolation.
The PK9210K has excellent noise performance for low light condition and high dynamic range (HDR) support using by DCG (Dual Conversion Gain) and multi- exposure method up to 120dB.

It incorporates on-chip CIS functions such as Defective Pixel Correction (DPC), Purple Fringing Reduction (PFR), exposure control, HDR combine reconstruction, and so on. It enables the PK9210K shows no saturation image in the worst contrast situations.
The PK9210K is suitable for a rear view camera and surround-view camera, home appliances and security applications with excellent image quality with 2.8V/1.8V/1.2V power supply.

Applications

- Rear View Camera
- 360° Surround View Monitoring System (SVM)
- Security
- Home appliances

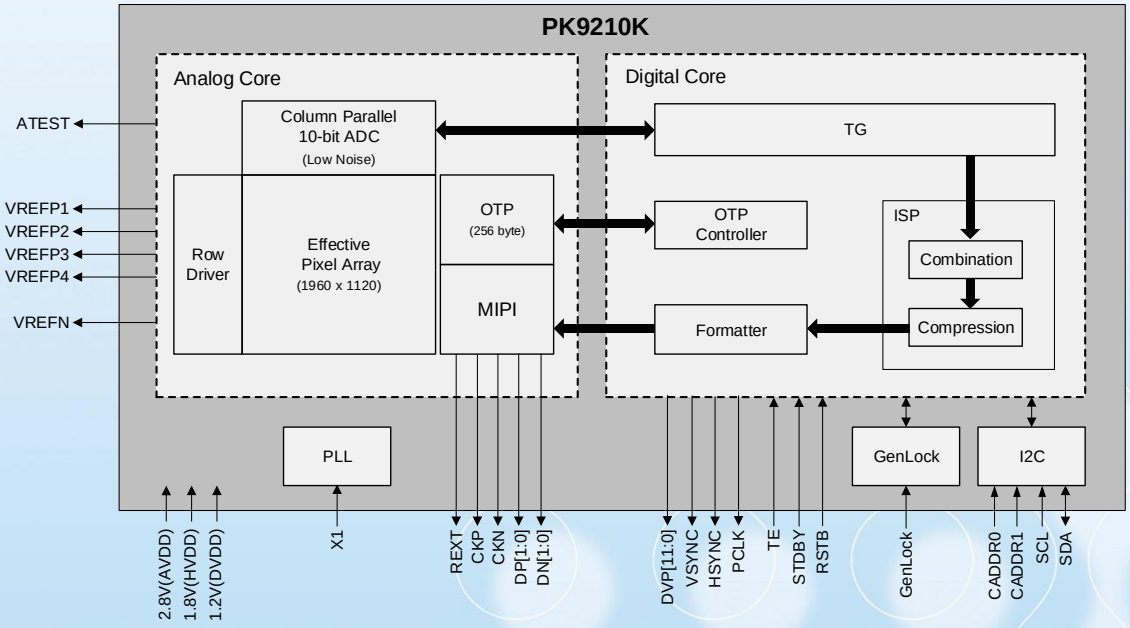
Product Features

- Support for display image size 1920 x 1080 with 2.0MP
- Support for HDR 120 dB with DCG and multi exposure.
- Support for combined RGB bayer output format
- ISP function : LSC, DPC, PFR, HDR combination, automatic black level correction, compression, etc
- Programmable frame size, window size, and exposure
- External synchronization support (Genlock)
- One-time programmable memory (OTP)
- Active Dummy Array for offset correction
- Spread Spectrum Clock Generation (SSCG)

Technical Specifications

Parameter	Typical value
Pixel size	2.8 um x 2.8 um
Effective pixel array	1960(H) x 1120(V)
Effective image area	5.4880 mm x 3.1360 mm
Optical format	1/2.92 inch
CRA	23.7 º
Input clock frequency	27 MHz
Output interface	2-Lane MIPI / DVP Combo
Max. frame rate	HDR 30 fps only
Dark Current	23 e-/sec @60℃
Sensitivity	30.3K e-/Lux. sec
Power supply	HVDD : 1.8 ~ 2.8V AVDD : 2.8 V DVDD : 1.2 V
Power consumption @30fps (HVDD = 1.8V / HVDD = 2.8V)	DPV : 204mW / 234mW MIPI : 201mW / 202mW Standby : 2mW /2mW
Operating temp.	-40 ~ 105 °C (Ambient)
Max. dynamic range	120 dB
SNR	44 dB @60℃
Package type	NeoPAC I / APLGA / 64CLCC
Package size(mm)	7.6 x 5.86 / 8.34 x 6.45 / 11.1 x 11.1

Functional Block Diagram



Crystal Image through Imaging **Innovation**

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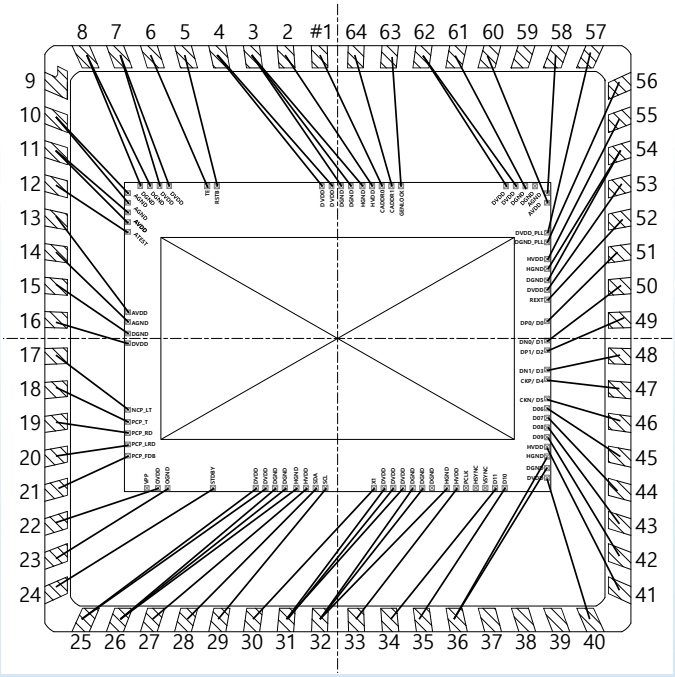
64CLCC Ball Map

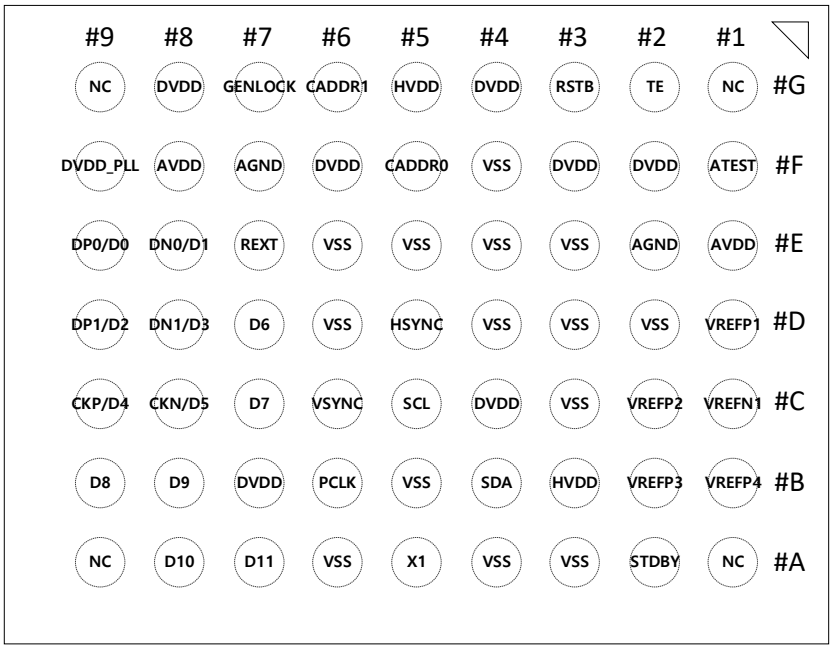


64CLCC Ball Description

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
1	CADDR0	I	pullup	Chip address bit 0
2	HVDD	P	-	IO VDD 1.8V~2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
3	HGND, DGND	P	-	IO GND / Digital(Core) GND
4	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
5	RSTB	I	pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
6	TE	I	pulldown	Chip test mode enable
7	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
8	DGND	P	-	Digital(Core) GND
9	AGND	P	-	Analog GND
10	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
11	ATEST	O	-	Analog test output
12	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
13	AGND	P	-	Analog GND
14	DGND	P	-	Digital(Core) GND
15	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
16	VREFN1	O	-	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
17	VREFP1	O	-	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
18	VREFP2	O	-	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
19	VREFP3	O	-	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
20	VREFP4	O	-	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
21	NC	-	-	-
22	NC	-	-	-
23	OVDD	P	-	Analog VDD 2.8V for OTP It should be tied with nearby OGND by 1uF bypass capacitors.
24	OGND	P	-	Analog GND for OTP
25	STDBY	I	pulldown	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither any beat of digital clock.
26	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
27	DGND, HGND	P	-	Digital(Core) GND / IO GND
28	HVDD	P	-	IO VDD 1.8V~2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
29	SDA	BIO	pullup	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor
30	SCL	BIO	pullup	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor
31	X1	I	pulldown	Master clock input pad
32	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
33	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby DGND by 1uF bypass capacitors.
34	DGND, HGND	P	-	Digital(Core) GND / IO GND
	HVDD	P	-	IO VDD 1.8V~2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
35	D11	O	pulldown	Digital Output bit 11
36	D10	O	pulldown	Digital Output bit 10
37	DGND, HGND	P	-	Digital(Core) GND / IO GND
38	NC	-	-	-
39	NC	-	-	-
40	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
41	HVDD	P	-	IO VDD 1.8V~2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
42	D9	O	pulldown	Digital Output bit 9
43	D8	O	pulldown	Digital Output bit 8
44	D7	O	pulldown	Digital Output bit 7
45	D6	O	pulldown	Digital Output bit 6
46	CKN/D5	O	pulldown	MIPI Clock Negative Output / Digital Output bit 5
47	CKP/D4	O	pulldown	MIPI Clock Positive Output / Digital Output bit 4
48	DN1/D3	O	pulldown	MIPI DN1 Output / Digital Output bit 3
49	DP1/D2	O	pulldown	MIPI DP1 Output / Digital Output bit 2
50	DN0/D1	O	pulldown	MIPI DN0 Output / Digital Output bit 1
51	DP0/D0	O	pulldown	MIPI DP0 Output / Digital Output bit 0
52	REXT	O	-	External Resistor for MIPI
53	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
54	DGND, HGND	P	-	Digital(Core) GND / IO GND
55	HVDD	P	-	IO VDD 1.8V~2.8V DC It should be tied with nearby HGND by 1uF bypass capacitors.
56	DGND_PLL	P	-	PLL GND
57	DVDD_PLL	P	-	PLL VDD 1.2V DC It should be tied with nearby DGND_PLL by 1uF bypass capacitors.
58	AGND	P	-	Analog GND
59	NC	-	-	-
60	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
61	DGND	P	-	Digital(Core) GND
62	DVDD	P	-	Digital(Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
63	GENLOCK	BIO	pulldown	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
64	CADDR1	I	pullup	Chip address bit 1

APLGA Ball Map

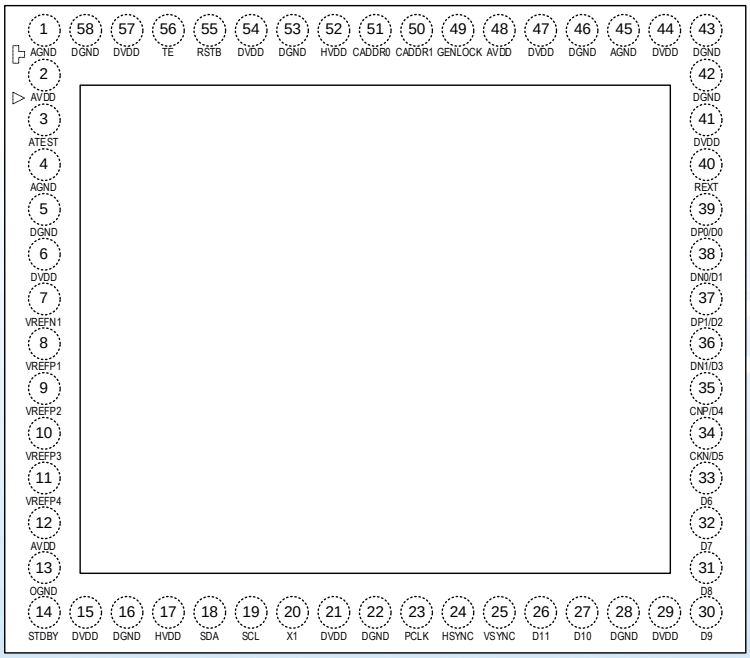


APLGA Ball Description

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
A2	STDBY	I	pulldown	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch , neither any beat of digital clock.
A3	VSS	P	-	Digital (Core) GND, IO GND
A4	VSS	P	-	Digital (Core) GND, IO GND
A5	X1	I	pulldown	Master clock input pad
A6	VSS	P	-	Digital (Core) GND, IO GND
A7	D11	O	pulldown	Digital Output bit 11
A8	D10	O	pulldown	Digital Output bit 10
B1	VREFP4	O	-	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.
B2	VREFP3	O	-	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
B3	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby DGND by 1uF bypass capacitors.
B4	SDA	BIO	pullup	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor
B5	VSS	P	-	Digital (Core) GND, IO GND
B6	PCLK	O	pulldown	PAD clock Data can be latched by external devices at the rising or falling edge of PCLK
B7	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
B8	D9	O	pulldown	Digital Output bit 9
B9	D8	O	pulldown	Digital Output bit 8
C1	VREFN1	O	-	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
C2	VREFP2	O	-	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
C3	VSS	P	-	Digital (Core) GND, IO GND
C4	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
C5	SCL	BIO	pullup	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor
C6	VSYNC	O	pulldown	Vertical sync : Indicates the start of a new frame
C7	D7	O	pulldown	Digital Output bit 7
C8	CKN/D5	O	pulldown	MIPI Clock Negative Output / Digital Output bit 5
C9	CKP/D4	O	pulldown	MIPI Clock Positive Output / Digital Output bit 4
D1	VREFP1	O	-	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
D2	VSS	P	-	Digital (Core) GND, IO GND
D3	VSS	P	-	Digital (Core) GND, IO GND
D4	VSS	P	-	Digital (Core) GND, IO GND
D5	HSYNC	O	pulldown	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
D6	VSS	P	-	Digital (Core) GND, IO GND
D7	D6	O	pulldown	Digital Output bit 6
D8	DN1/D3	O	pulldown	MIPI DN1 Output / Digital Output bit 3
D9	DP1/D2	O	pulldown	MIPI DP1 Output / Digital Output bit 2
E1	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by 1uF bypass capacitors.
E2	AGND	P	-	Analog GND
E3	VSS	P	-	Digital (Core) GND, IO GND
E4	VSS	P	-	Digital (Core) GND, IO GND
E5	VSS	P	-	Digital (Core) GND, IO GND
E6	VSS	P	-	Digital (Core) GND, IO GND
E7	REXT	O	-	External Resistor for MIPI
E8	DN0/D1	O	pulldown	MIPI DN0 Output / Digital Output bit 1
E9	DP0/D0	O	pulldown	MIPI DP0 Output / Digital Output bit 0
F1	ATEST	O	-	Analog test output
F2	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
F3	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
F4	VSS	P	-	Digital (Core) GND, IO GND
F5	CADDR0	I	pullup	Chip address bit 0
F6	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
F7	AGND	P	-	Analog GND
F8	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by 1uF bypass capacitors.
F9	DVDD_PLL	P	-	PLL VDD 1.2V DC It should be tied with nearby DGND_PLL by 1uF bypass capacitors
G2	TE	I	pulldown	Chip test mode enable
G3	RSTB	I	pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
G4	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G5	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby DGND by 1uF bypass capacitors.
G6	CADDR1	I	pullup	Chip address bit 1
G7	GENLOCK	BIO	pulldown	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
G8	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.

NeoPAC I Ball Map



NeoPAC I Ball Description

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
1	AGND	P	-	Analog GND
2	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by 1uF bypass capacitors.
3	ATEST	O	-	Analog test output
4	AGND	P	-	Analog GND
5	DGND	P	-	Digital (Core) GND
6	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
7	VREFN1	O	-	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
8	VREFP1	O	-	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
9	VREFP2	O	-	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
10	VREFP3	O	-	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
11	VREFP4	O	-	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.
12	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by 1uF bypass capacitors.
13	OGND	P	-	Analog GND for OTP
14	STDBY	I	pulldown	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither a ny beat of digital clock.
15	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
16	DGND	P	-	Digital (Core) GND
17	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby DGND by 1uF bypass capacitors.
18	SDA	BIO	pullup	2-wire serial interface clock, SDA line is pulled up to HVDD by off-chip resistor
19	SCL	BIO	pullup	2-wire serial interface data, SCL line is pulled up to HVDD by off-chip resistor
20	X1	I	pulldown	Master clock input pad
21	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
22	DGND	P	-	Digital (Core) GND

Ball	Ball Name	IO	Pull up/ Pull down	Ball Description
23	PCLK	O	pulldown	PAD clock Data can be latched by external devices at the rising or falling edge of PCLK
24	HSYNC	O	pulldown	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
25	VSYNC	O	pulldown	Vertical sync : Indicates the start of a new frame
26	D11	O	pulldown	Digital Output bit 11
27	D10	O	pulldown	Digital Output bit 10
28	DGND	P	-	Digital (Core) GND
29	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
30	D9	O	pulldown	Digital Output bit 9
31	D8	O	pulldown	Digital Output bit 8
32	D7	O	pulldown	Digital Output bit 7
33	D6	O	pulldown	Digital Output bit 6
34	CKN/D5	O	pulldown	MIPI Clock Negative Output / Digital Output bit 5
35	CKP/D4	O	pulldown	MIPI Clock Positive Output / Digital Output bit 4
36	DN1/D3	O	pulldown	MIPI DN1 Output / Digital Output bit 3
37	DP1/D2	O	pulldown	MIPI DP1 Output / Digital Output bit 2
38	DN0/D1	O	pulldown	MIPI DN0 Output / Digital Output bit 1
39	DP0/D0	O	pulldown	MIPI DP0 Output / Digital Output bit 0
40	REXT	O	-	External Resistor for MIPI
41	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
42	DGND	P	-	Digital (Core) GND
43	DGND	P	-	PLL GND
44	DVDD	P	-	PLL VDD 1.2V DC It should be tied with nearby DGND_PLL by 1uF bypass capacitors.
45	AGND	P	-	Analog GND
46	DGND	P	-	Digital (Core) GND
47	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
48	AVDD	P	-	Analog VDD 2.8V It should be tied with nearby AGND by 1uF bypass capacitors.
49	GENLOCK	BIO	pulldown	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
50	CADDR1	I	pullup	Chip address bit 1
51	CADDR0	I	pullup	Chip address bit 0
52	HVDD	P	-	IO VDD 1.8V ~ 2.8V DC It should be tied with nearby DGND by 1uF bypass capacitors.
53	DGND	P	-	IO GND
54	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
55	RSTB	I	pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
56	TE	I	pulldown	Chip test mode enable
57	DVDD	P	-	Digital (Core) VDD 1.2V DC It should be tied with nearby DGND by 1uF bypass capacitors.
58	DGND	P	-	Digital (Core) GND